



Attorney Docket No. 5646-81

FW
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Proebsting et al.
Serial No.: 10/643,208
Filed: August 18, 2003
For: INTEGRATED CIRCUIT DEVICES HAVING PRECISION DIGITAL DELAY LINES
THEREIN

Group Art Unit: 2812
Examiner: To Be Assigned
Confirmation No.: 4050

Date: August 11, 2004

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on Form PTO-1449, together with a copy of any listed foreign patent document and/or non-patent literature. A copy of any listed U.S. patent and/or U.S. patent application publication is not provided herewith in accordance with the waiver by the U.S. Patent and Trademark Office of requirements under 37 C.F.R. § 1.98(a)(2)(i) for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003.

It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

[Signature]
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 11, 2004.

[Signature]
Candi L. Riggs

Serial No.
10/643.208

LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

Applicants: Proebsting et al.

Filing Date: August 18, 2003

Group
2812

U. S. PATENTS & PATENT APPLICATION PUBLICATIONS

[illegible]

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	5	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496

DATE CONSIDERED

*EXAMINER

Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.